FULL VERSION OF PENDING CLAIMS:

Claims 1 - 28 (cancelled)

Claim 29 (previously added): A processor for executing an instruction sequence generated by converting a program that is capable of being described by mutually exclusive first and second conditional instructions, so that the instruction sequence includes only the first conditional instruction out of the first and second conditional instructions,

wherein the processor has only the first conditional instruction out of the first and second conditional instructions.

Claim 30 (previously added): The processor of Claim 29,

wherein the first conditional instruction is a conditional transfer instruction.

Claim 31 (previously added): The processor of Claim 29,

wherein the first conditional instruction is a conditional arithmetic instruction.

Claim 32 (previously added): A processor for executing an instruction sequence generated by converting a program that is capable of being described by mutually exclusive first and second conditional instructions, so that the instruction sequence includes only the first conditional instruction out of the first and second conditional instructions,

wherein the processor is operable to decode only the first conditional instruction out of the first and second conditional instructions.

Claim 33 (currently amended): The processor of Claim 32,

wherein the first conditional instruction is a conditional transfer instruction.

Claim 34 (currently amended): The processor of Claim 32,

wherein the first conditional instruction is a conditional arithmetic instruction.

Claim 35 (previously added): A processor for executing an instruction sequence generated by converting a program that is capable of being described by mutually exclusive first and second conditional instructions, so that the instruction sequence includes only the first conditional instruction out of the first and second conditional instructions,

wherein the processor is operable to execute only the first conditional instruction out of the first and second conditional instructions.

Claim 36 (currently amended): The processor of Claim 35,

wherein the first conditional instruction is a conditional transfer instruction.

Claim 37 (currently amended): The processor of Claim 35,

wherein the first conditional instruction is a conditional arithmetic instruction.

Claim 38 (currently amended): A processor that executes an instruction sequence, comprising:

a decoding unit operable to decode an instruction sequence generated by converting a program that is capable of being described by mutually exclusive first and second conditionally instructions, so that the instruction sequence includes only the first conditional instruction out of the first and second conditional instructions; and

an executing unit operable to execute the instruction sequence decoded by the decoding unit;

wherein the decoding unit is operable to decode only the first conditional instruction out of the first and second conditional instructions.

Claim 39 (currently amended): An instruction conversion apparatus for converting a program that is capable of being described by mutually exclusive first and second conditional instructions into an instruction sequence executable by a processor,

wherein the instruction conversion apparatus, when only the first conditional instruction out of the first and second conditional instructions is decodable by the processor, interchanges (a) a condition of the second conditional instruction with a condition of the first conditional instruction, and (b) an instruction executed when the condition of the second conditional instruction is satisfied with an instruction executed when the condition of the second conditional instruction is ~~satisfied with an instruction executed when the condition of the second conditional instruction is~~ not satisfied.

Claim 40 (currently amended): An instruction conversion apparatus, comprising:

an intermediate code generating unit operable to generate an intermediate code sequence by converting a program that is capable of being described by mutually exclusive first and second conditional instructions;

a detecting unit operable to detect, from the intermediate code sequence, (a) a conditional instruction that judges whether to execute one of a first operation and a second operation, (b) a first operation code that executes an instruction when the judgment result of the conditional instruction is to execute the first operation, and (c) a second operation code that executes an instruction when the judgment result of the conditional instruction is to execute the second operation; and

an interchanging unit operable, when only the first conditional instruction out of the first and second conditional instruction is decodable by a processor, to interchange (a) the second conditional instruction with the first conditional instruction, and (b) an operation of the first operation with an operation of the second operation.

REMARKS

Claims 33-34, and 36-40 are amended to correct typographical errors. Applicant respectfully requests this amendment be entered prior to examination on the merits.

If the Examiner believes that a telephone interview will help further the prosecution of this case, the Examiner is respectfully requested to contact the undersigned attorney at the listed telephone number.

I hereby certify that this document and fee is being deposited on August 6, 2003 with the U.S. Postal Service as first class mail under 37 C.F.R. §1.8 and is addressed to Mail Stop Patent Application Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.

By: James Lee

Signature

Date of Signature: August 6, 2003

Very truly yours,

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